Microstructural Control of Charge Transport in Organic Blend Thin-Film Transistors

*Simon Hunter, Jihua Chen, and Thomas D. Anthopoulos**

The charge-transport processes in organic p-channel transistors based on the small-molecule 2,8-difluoro-5,11-bis(triethylsilylethynyl)anthradithiophene (diF-TES ADT), the polymer poly(triarylamine)(PTAA) and blends thereof are investigated. In the case of blend films, lateral conductive atomic force microscopy in combination with energy filtered transmission electron microscopy are used to study the evolution of charge transport as a function of blends composition, allowing direct correlation of the film's elemental composition and morphology with hole transport. Low-temperature transport measurements reveal that optimized blend devices exhibit lower temperature dependence of hole mobility than pristine PTAA devices while also providing a narrower bandgap trap distribution than pristine diF-TES ADT devices. These combined effects increase the mean hole mobility in optimized blends to 2.4 cm^2/Vs – double the value measured for best diF-TES ADT-only devices. The bandgap trap distribution in transistors based on different diF-TES ADT:PTAA blend ratios are compared and the act of blending these semiconductors is seen to reduce the trap distribution width yet increase the average trap energy compared to pristine diF-TES ADT-based devices. Our measurements suggest that an average trap energy of <75 meV and a trap distribution of <100 meV is needed to achieve optimum hole mobility in transistors based on diF-TES ADT:PTAA blends.

1. Introduction

In recent years the performance of organic transistors has increased markedly; something that has been achieved by two separate approaches. The first has involved cleverer synthetic design of polymer semiconductors, resulting in materials with mobility of up to 12 cm^2/Vs in thin film transistors (TFTs).[1–5] However, high annealing temperatures of up to 200 °C are commonly needed, and the increasing complexity of these polymeric semiconductors makes them less suitable to industrial scale synthesis. The second approach has involved developing new processing methods to control the crystallisation of small molecule organic semiconductors. Techniques such as solution shearing, which involves applying strain to the film as it crystallises, has been shown to increase the molecular packing density and increase carrier mobility up to 11 cm^2/Vs;[6,7] inkjet printed TFTs deposited using a dual solvent method have also shown improved molecular ordering, with average hole mobilities of 16 cm^2/Vs;[8] and even spin coating techniques have demonstrated TFTs with exceedingly high mobilities of over 40 cm^2/Vs.[9] Finally, blending a small molecule semiconductor with an amorphous, conjugated polymer has also been shown to provide increased control over crystal formation through managing vertical phase separation of the two components.[10–16] This method has yielded TFTs with carrier mobilities of over 5 cm^2/Vs and isn't reliant on the use of complex polymer semiconductors, while providing simpler processing than using small molecule semiconductors alone.[12] Additionally, and importantly, this impressive performance is observed as being independent of the film microstructure, enabling a wide processing window for TFTs fabricated from semiconductor blends at plastic compatible temperatures (<120 °C).[17] A recent review article by Noh et al. discusses many of the advances in organic semiconductor processing methods and discusses them in the context of fabricating printed integrated circuits: one of the ultimate goals for the field.[18]

In these blend systems the small molecule component is responsible for achieving high charge carrier mobility while the polymer binder is required for forming smooth, uniform films. The blend films can be deposited from a solution with a high boiling-point solvent using different techniques including; spin-casting,[13] ink-jet printing[15] or bar-coating.[19,20] Once deposited, the film is still liquid and by managing the rate of subsequent solvent removal the film's final microstructure can be controlled. Typically, this means achieving strong vertical phase separation such that the air/film interface is dominated by a crystalline small molecule layer. Therefore, a top-gate transistor architecture (**Figure 1**a) can be employed to take

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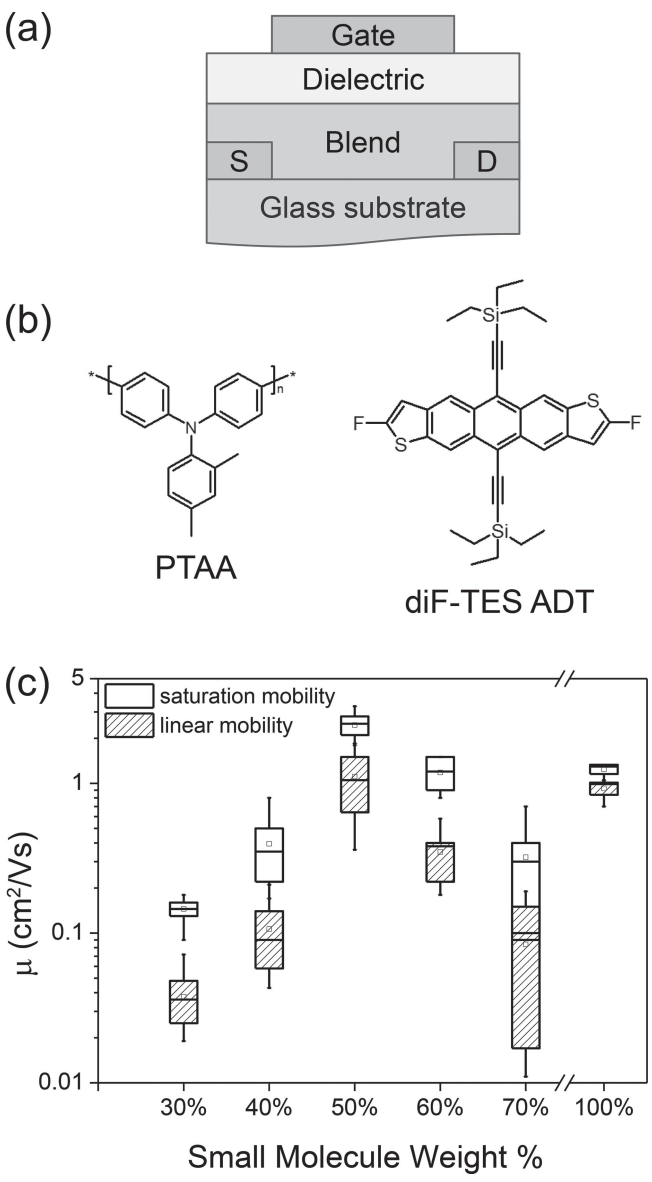

Figure 1. (a) Cartoon depicting the top-gate bottom-contact TFT architecture used for the devices in this study. Phase separation ensures the small molecule diF-TES ADT forms at the interface between the blend and the dielectric, while the polymer PTAA is the primary constituent in the bulk. (b) Chemical structures of the polymer and small molecule semiconductors used in this study. (c) Plot depicting saturation and linear mobility versus blend composition of at least 10 devices at each diF-TES ADT weight%.

advantage of the crystalline and high carrier mobility film/air interface.

While considerable work has been conducted on organic TFTs based on a blend of semiconductor components, there has been relatively little work done to obtain a greater understanding of the underlying charge transport through such blend films and devices. In order to be able to design improved blend TFTs it is important to understand how variations in the composition of the semiconductor film affects device performance. Smith et al. studied the percolation behaviour of charge carriers through blend TFTs based on 2,8- difluoro-5,11-bis(triethylsilylethynyl) anthradithiophene (diF-TES ADT) and poly(triarylamine) (PTAA), both p-type organic semiconductors, with different relative compositions.[10] They found that the critical diF-TES ADT concentration required for percolation pathways to form was 39 wt.%, and above 60 wt.% increasing film roughness lead to a reduction in device performance. Li et al. conducted a similar study on blends of 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-pentacene) and polystyrene, finding that for bottom gate transistors a higher concentration of the small molecule component (80 wt.%) was necessary for maximum hole mobility in a TFT.[15]

In this work we have studied the evolution of hole transport in semiconducting diF-TES ADT : PTAA blend films and devices[21] using a range of complementary techniques. The chemical structures of diF-TES ADT and PTAA are shown in Figure 1b. Nano-scale lateral conductivity mapping measurements have been performed on blend films with a range of compositions, above, below and at the percolation threshold. Obtained results allowed, for the first time, direct visualisation of the hole conduction pathways through the blend films as a function of blend composition and the resulting film morphology. Furthermore, low temperature charge transport measurements were conducted on blend TFTs in order to evaluate the effect of varying the blend composition on the charge transport mechanism. From this we show that an optimized blend ratio provides a minimum average trap energy, thereby allowing a greater proportion of induced charges to be mobile. We show that the evolution of trap states in organic semiconducting blend films of different relative compositions is directly related with the morphology of the semiconducting channel. Finally, we demonstrate, for the first time, the direct effects bandgap trap distributions have on device performance in these blend devices, laying out requirements for further improvements.

2. Theory

Usually, the charge carrier mobility in a TFT is extracted using the MOS-FET model which states that the linear and saturation mobilities are given by:

$$\mu_{\text{lin}} = \frac{L}{WC_iV_D}\frac{\partial I_{D,\text{lin}}}{\partial V_G} \quad (1)$$

$$\mu_{\text{sat}} = \frac{L}{WC_i}\frac{\partial^2 I_{D,\text{sat}}}{\partial V_G^2} \quad (2)$$

In the above expressions L is the channel length, W is the channel width, C_i is the geometric capacitance, V_D is the drain voltage, I_D is the current flowing between source and drain electrodes, and V_G is the gate voltage. However, in many systems this model tends to overestimate the carrier mobility at low to moderate V_G, while providing a decreasing mobility at high V_G.[16,22] This is unphysical as it has been widely shown that carrier mobility in these relatively disordered organic systems increases monotonically with carrier density.[23–26] As such, for the temperature measurements we conducted, the mobility was

extracted from the linear regime using an effective mobility calculation that averages over mobile and trapped charges. This is done by setting the threshold voltage to zero, $V_T = 0$, and is suitable for systems dominated by charge trapping and exhibiting thermally activated mobility.[21,27] The resulting equation is given by:

$$\mu_{\text{ff}} = \frac{L}{WC_iV_D}\frac{I_{D,\text{lin}}}{(V_G - V_{\text{on}})} \tag{3}$$

where μ_{eff} is the linear regime effective hole (LREH) mobility, V_{on} is the onset voltage, which at room temperature is approximately zero but becomes increasingly negative at lower temperatures (see Supporting Information).

The transport of carriers through disordered semiconductors is usually modelled using an Arrhenius relationship, which describes a temperature activated mobility, such that:

$$\mu_{\text{eff}} \approx \mu_0 \exp\left(-\frac{E_A}{k_BT}\right) \tag{4}$$

Here, E_A is the activation energy of the measured carrier mobility, which can be considered as the characteristic trap position, relative to the transport level i.e. $E_A = E_T - E_V$, where E_T is the trap energy, E_V is the energy of the transport level, and μ_0 is a mobility prefactor. However, the reality of disordered systems means that no such single trap level exists, but rather it is better to model the trap states as an exponential distribution of band-tail states. This multiple trapping and release (MTR) interpretation means that E_A is no longer a discrete energy, but instead is a function of V_G. This is because as the gate bias increases, so does the Fermi level, filling trap states and reducing the characteristic trap depth. Under this condition, it is appropriate to apply the Meyer-Neldel Rule (MNR). The MNR, when applied to electrical conduction, describes the carrier mobility as a function of gate-bias and predicts a temperature at which this dependence of mobility on gate bias disappears; the so-called iso-kinetic temperature, T_0.[28,29] The width of the trap distribution can then be estimated from the Meyer-Neldel energy, k_BT_0, which is calculated from an extended Arrhenius equation:

$$\mu_{\text{eff}} = \mu_{00} \exp\left(-\frac{E_A}{k_BT} + \frac{E_A}{k_BT_0}\right) \tag{5}$$

3. Results & Discussion

A minimum of ten diF-TES ADT:PTAA based TFTs were fabricated for each blend composition between 30–70 wt.% with steps of 10 wt.%. The resulting devices exhibited hole mobilities that peaked at 50 wt.% with a mean value of 2.4 ± 0.4 cm^2/Vs (saturation) and 1.1 ± 0.5 cm^2/Vs (linear), taking the estimated standard deviation as the error (Figure 1c – further figures of merit for the blend devices fabricated in this study are found in Table S1). As expected, the 50 wt.% blend devices performed the best in agreement with previous work conducted by Smith et al.[10] The hole mobility measured from these optimised devices was among the highest ever measured using the diF-TES ADT semiconductor, with most deposition methods resulting in devices with mobility values an order of magnitude lower.[30] Only single crystal diF-TES ADT TFTs have been shown to consistently outperform those fabricated in this study.[31] Blend films with small molecule compositions below 30 wt.%, however, exhibited no visible phase-separated crystallisation (observed using polarized optical microscopy), whereas increasing the ratio to 50 wt.% resulted in continuous crystal coverage.

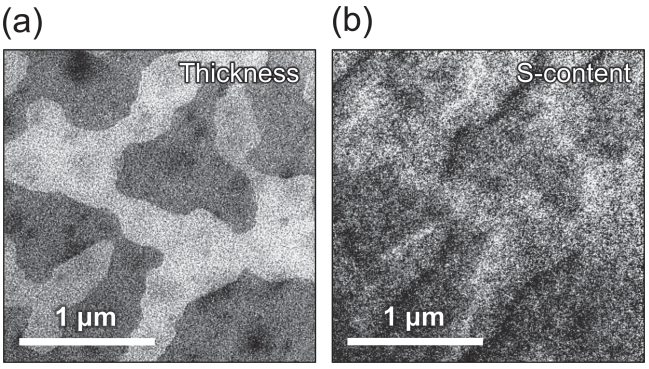

Figure 2. Thickness (a) and sulphur (b) EF-TEM maps of a 30 wt.% blend film. The brighter regions in the S-content map correspond to a greater concentration of the sulphur-containing diF-TES ADT.

Energy-filtered transmission electron microscopy (EF-TEM) was also conducted on blend films to highlight the microstructure evolution with compositional variation. 10 wt.% and 20 wt.% blend films exhibit no obvious phase separation either in thickness or composition (Figure S2). As the diF-TES ADT component is sulphur-rich it appears brighter in the sulphur maps and therefore the crystalline small molecule regions are lighter than the surrounding matrix. Hence, as can be seen in **Figure 2**, the islands are indeed diF-TES ADT crystals, surrounded by a mixed phase of the polymer and small molecule component (a persistent background signal for S exists in all EF-TEM measurements).

To rationalise the observed TFT performance with analysis of the microstructure and conduction pathways through the semiconducting blend channel, lateral conductive-atomic force microscopy (C-AFM) was performed. This technique involves scanning a metal-coated AFM probe at a lateral distance from a biased electrode; as such it allows the simultaneous visualisation of topography (**Figure 3**a) and conductivity of the semiconducting film (Figure 3b) in the TFT channel, at the semiconductor-dielectric interface.[17] 30 wt.% films exhibit small crystals with varying degrees of interconnection (an area exhibiting relatively high interconnectivity is shown in Figure 3b, 30 wt.% image). The continuity of crystal structures across a transistor channel is vital to ensure percolation of charge carriers through the high mobility small molecule. As can be seen in Figure 3 (30 wt.%), isolated crystals in the upper left of the map exhibit lower conductivity than the connected crystals. Increasing the small molecule concentration to 40 wt.% leads to the formation of larger crystals which provide fully connected percolation pathways through the film (Figure 3b, 40 wt.% image). As such, the conductivity of these surface crystals increases relative to the mixed polymer phase

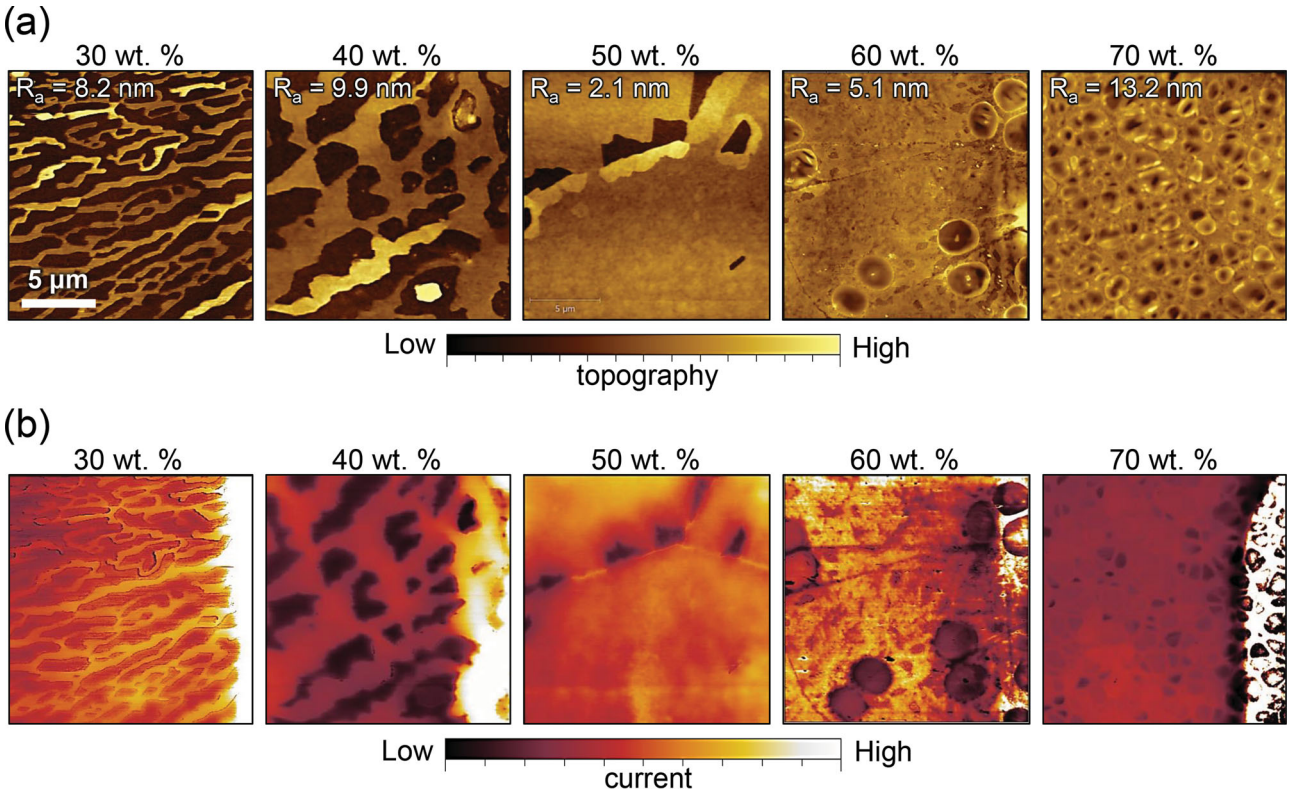

Figure 3. AFM topography (a) and corresponding lateral current maps of 30 – 70 wt.% diF-TES ADT:PTAA blend films (b). In (b) the remote biased electrode is located to the right of each map. Increasing the loading of the small diF-TES ADT component leads to increased film roughness and lower conductivity. The current scale is normalised to eliminate variations in the conductive coating of the AFM probe between samples. As a result similar region coloration between different images does not imply similar conductivities.

beneath them. While this increase in conductivity through the crystals relative to the underlying mixed phase is considerable, it should be noted that the relative conductivity is likely not indicative of the two components in a functioning TFT, where the transconductance of the two components is likely to be different. The formation of these percolation pathways is responsible for a median saturation mobility increase of over 100% in top-gate TFTs.

At a 50 wt.% composition the film exhibits an entirely crystalline upper layer, excepting the occasional perforation (Figure 3, 50 wt.% images). This leads not only to increased device performance but also to a lower parameter spread (Figure 1) due to the more homogenous crystal surface of the film. Increasing the loading fraction of diF-TES ADT beyond 50 wt.% causes cratering of the crystal surface. These craters (which are composed of crystalline diF-TES ADT) not only increase the roughness of the semiconductor surface (surface RMS roughness of the 70 wt.% blend film is ~12 nm vs. <2 nm for a continuous crystal in the 50 wt.% film) but the craters are also considerably electrically insulating (Figure 3, 60–70 wt.% images). The formation of these craters in the 60 wt.% films is probably due to localised regions which are heavily saturated with diF-TES ADT molecules and upon drying lead to homogenous crystallisation.[32] Such crystallisation then becomes dominant in regions of 70 wt.% films, creating the disordered microstructure seen in Figure 3 for >60 wt.%. Homogenous crystallisation prevents the extended molecular ordering seen in the optimized blends and therefore the carrier mobility drops. The competition between homogenous and heterogeneous crystallisation that occurs during drying of these high diF-TES ADT wt.% films leads to a significant increase in the device parameter spread as seen in Figure 1.

In order to obtain a greater understanding of the structure-property relationship in these blend films, the electronic properties of as-prepared TFTs were tested as a function of temperature of between 130 and 320 K. This allowed the combined gate field doping and temperature dependence of hole mobility to be studied using the same set of devices. 3D surface plots of the temperature and gate voltage dependence of the LREH mobility are shown in Figure S2. The single-component PTAA devices showed strong temperature dependence, with transport practically frozen out (i.e., low activation energy – E_A) below 180 K. This contrasts with the single-component diF-TES ADT device which demonstrated balanced dependence of the carrier mobility on both gate bias and temperature.

As the concentration of diF-TES ADT in the blend is increased, two trends become apparent: Below the optimized 50 wt.% composition, charge transport at low temperatures becomes increasingly efficient until the low-T performance of the 50 wt.% blend matches that of the pristine diF-TES ADT device, i.e., $\mu(130\mathbf{K}) = \frac{1}{4}\mu(320\mathbf{K})$. Therefore, the low-T performance of the blend devices is determined by the fraction of the channel that is composed of crystalline small molecule. This property arises from the differences in charge transport

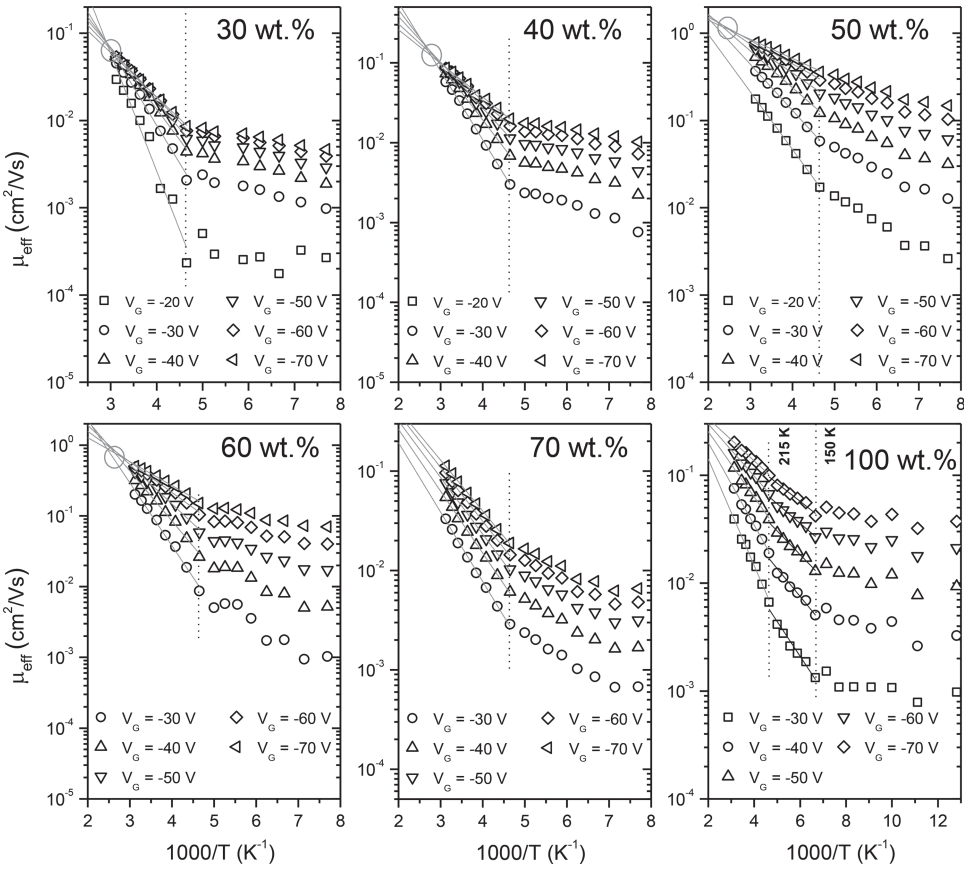

Figure 4. Arrenhius plots of the LREH mobility of compositionally different blend TFTs and single-component diF-TES ADT TFT conducted at various gate voltages. Where the Meyer-Neldel rule is obeyed the location of kT_0 is circled. Common to all the devices is the transition temperature of approximately 215 K.

through the amorphous polymer and crystalline small molecule components. The close packing of diF-TES ADT molecules, and hence low energetic disorder, contrasts with the lower electronic overlap of adjacent conjugated units in amorphous polymers.[24] This results in charge transport that exhibits much greater temperature dependence (higher E_A) through the PTAA component than through the crystalline diF-TES ADT. The second trend that is apparent is how the gate bias dependence of hole mobility changes as the loading fraction of diF-TES ADT is increased above 50 wt.%. Below the optimized ratio carrier mobility saturates at high gate bias, however above 50 wt.% the carrier mobility increases monotonically. This is evidence of a change in the trap distribution in the channel due to the film surface becoming increasingly disordered.

Arrhenius plots of LREH mobility were constructed for the different blend compositions as well as devices using the single component semiconductors (**Figure 4**). All blend devices exhibited two temperature-dependent transport regimes, with greater temperature dependence of mobility at T > 215 K. This critical temperature was also observed in the single-component PTAA device, but was much less significant in the pristine diF-TES ADT device. The mobility prefactor, μ_0, was extracted from the Arrhenius plots and compared between the blend devices with a ratio of ≥40 wt.% diF-TES ADT (i.e. above the percolation limit). This resulted in a consistent prediction of LREH mobility at infinite temperature of 2–6 cm^2/Vs. The pristine diF-TES ADT film, however, predicts a maximum of 0.8 cm^2/Vs. This further suggests that the act of using a small molecule semiconductor in a blend is able to fundamentally improve the charge transport compared to the pristine small molecule based films. To maximise this benefit, however, the morphology must be further optimised.

The Arrhenius plots were used to extract the activation energy (E_A) in the high temperature regime (> 215K) as described in Equation (4) and this was plotted as a function of carrier density, gate bias and blend composition in **Figure 5**. The induced carrier density was estimated from the gate bias above V_{on} and includes both mobile and trapped charges. While this approximation assumes that induced carriers form a 2D charge layer, in reality the low permittivity of organic semiconductors means that the carriers occupy a layer several nm thick. Since E_A may be regarded as the characteristic trap location relative to the transport level, it may also serve as a measure of the temperature-dependence of carrier mobility in the semiconductor layer. The single component devices (0 wt.% and 100 wt.%) exhibit relatively low activation energies, with the PTAA device also displaying gate bias (and therefore carrier density) independent E_A. In contrast, devices fabricated using an imbalanced blend of semiconductor components show greatly increased activation energies with a strong gate bias dependence. This demonstrates

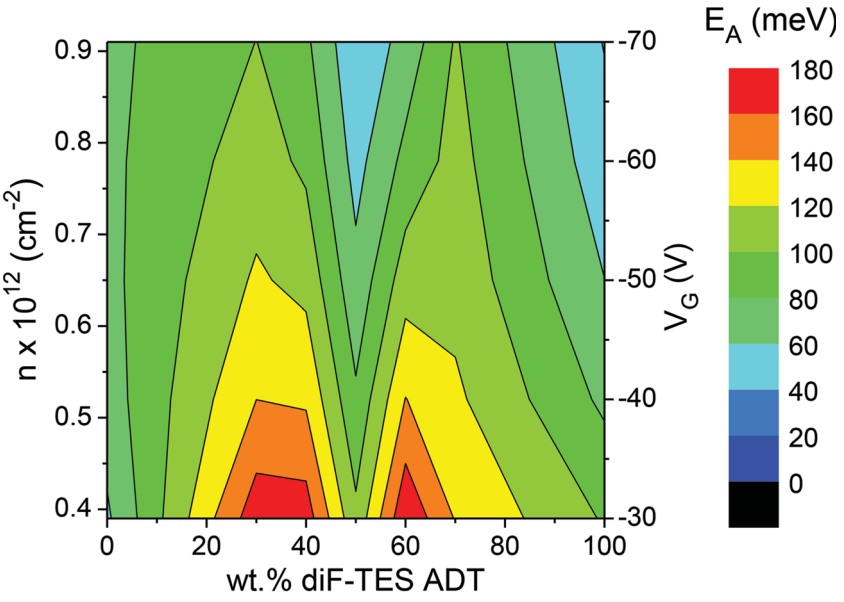

Figure 5. Contour plot of the activation energy (E_A) for charge transport in compositionally different films at different gate biases (V_G). Also added for comparison is the induced carrier density, including both mobile and trapped charges.

that blending different semiconducting components has the potential to greatly increase the density of charge traps in the transistor channel. Importantly however, the balanced blend ratio of 50 wt.% diF-TES ADT represents a local minimum of E_A, clearly demonstrating the importance of achieving an optimized composition. Additionally, while the 70 wt.% and 100 wt.% diF-TES ADT devices both exhibit a relatively disordered surface morphology (which is most probably composed entirely of the small molecule), the 70 wt.% device has a much larger E_A. This shows that while the polymer matrix component likely provides very little in terms of charge transport through the TFT channel, it still influences the ultimate performance of the device. The origin of this behaviour is believed to arise from charge injection and extraction to and from the crystalline channel, which occurs through a mixed phase of PTAA and diF-TES ADT. The high E_A of the PTAA will contribute to a similar increase in the activation energy of the 70 wt.% blend. This analysis shows that by producing a non-optimized blend the average trap energy is significantly deeper within the bandgap than when it is optimized. For instance, with $V_G = -70$ V, E_A = 43 meV for the optimized blend, but rises to ~100 meV and ~102 meV for the 30 wt.% and 70 wt.% blends, respectively.

To gain a greater understanding of the trap distribution in the various blend TFTs, the MNR was used. As PTAA devices exhibited a constant temperature-dependence of carrier mobility (i.e. the slope of $\ln(\mu_{eff})$ against $\frac{1}{T}$ exhibits no V_G dependence for $V_G > |-40|$ V – Figure S4), it can be modelled as having a discrete trap state, with a depth, $E_T - E_V = 75$ meV.[28] Thus, the PTAA TFT demonstrated no iso-kinetic temperature making the MNR inapplicable in this situation. However, for all the blend devices, and the single component diF-TES ADT devices, an iso-kinetic temperature was observed as well as a $\ln(\mu_0) \propto E_a$ relationship, demonstrating that the Meyer-Neldel rule is obeyed. The values of kT_0 for the blend devices with compositions between 30 and 60 wt.% diF-TES ADT, were found to be in the range $25 < kT_0 < 40$ meV, without any strong correlation to blend composition. These values are consistent with results seen for other organic semiconductor systems[29,33,34] as well as various disordered inorganic semiconductors such as hydrogenated amorphous silicon[35] and chalcogenide glasses,[36] possibly suggesting that the source/origin of the activation energy is similar in all of these systems.

Despite this, quite contradictory results were seen for both the 70 wt.% blend and pristine diF-TES ADT devices. The diF-TES ADT TFT exhibited a Meyer-Neldel energy of 110 ± 10 meV, while the 70 wt.% blend devices showed exceptionally weak gate bias dependence of E_A leading to a calculated Meyer-Neldel energy of 350 ± 70 meV (**Figure 6**). This is exceedingly high and, to the best of the author's knowledge, no equivalent values have been measured in organic semiconducting systems. These high kT_0 values demonstrate the considerable energetic disorder in these high diF-TES ADT wt.% films based devices, highlighting the consequences of not achieving controlled crystallisation of the small molecule.

The Meyer-Neldel energies of all film compositions studied are plotted on the semi-logarithmic plot vs. E_A in Figure 6. From this plot, one can clearly see the effect that blending of the two semiconducting components has on the energetic distribution of bandgap states within the semiconducting channel. Firstly, using PTAA as a binder to control crystallisation of the diF-TES ADT aids in narrowing the trap distribution. This reduces the subthreshold swing and threshold voltage (see supporting information). While this is beneficial, pristine diF-TES ADT exhibits a surprisingly low characteristic trap energy and blending the two components increases this average trap energy. As both trap depth and energetic distribution have an effect on the number of mobile carriers in the channel for a given gate bias, improvements in device performance (i.e., increased hole mobility) are only achieved when both of these parameters are minimized. In Figure 6, an area is shaded to highlight the properties of bandgap states our results have empirically indicated are required to achieve devices with increased mobility over TFTs employing the pristine small molecule semiconductor. The 50 wt.% device falls well within this region and consequently exhibits improved device performance over the pristine diF-TES ADT devices, i.e., increased carrier mobility and reduced subthreshold swing and threshold voltage. The 60 wt.% device falls on the edge of this region as its performance is approximately equal to that of the single component devices (Figure 1). Note that the characteristic trap depth of PTAA is also added to Figure 6 for comparison but does not fall under the same analysis as it is devoid of the small molecule component.

The origin of the hole trap states in this system is difficult to ascertain. While it appears fairly obvious that increased morphological disorder in the films increases the trap density,

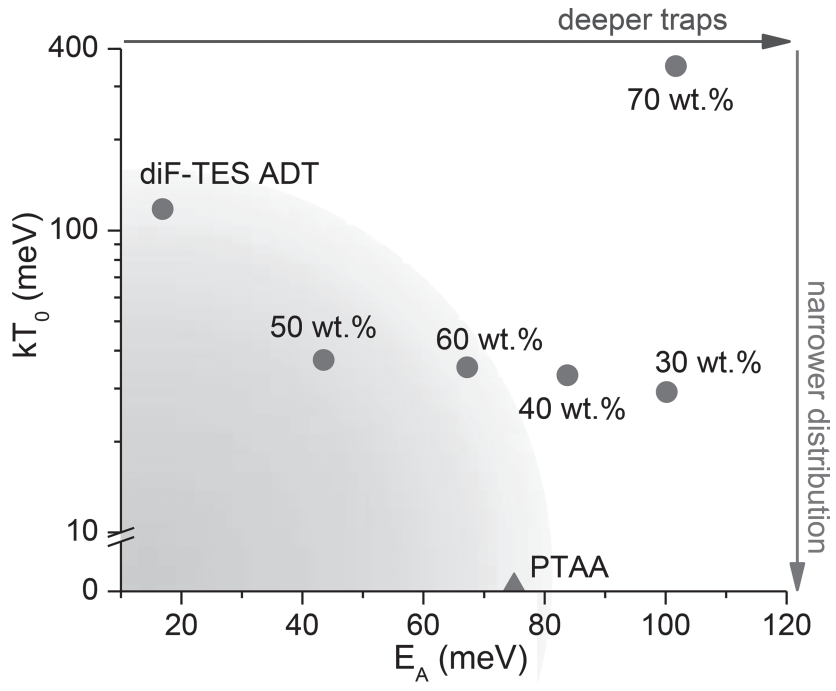

Figure 6. Plot depicting the characteristics of bandgap trap distributions in both blended and single component devices. The shaded region demonstrates the necessary parameters for improved device performance over the single component diF-TES ADT. The activation energy (E_A) for PTAA is added for comparison although does not exhibit a Meyer-Neldel energy.

it is not possible within the analysis conducted here to confidently predict the various contributions. Grain boundaries, crystal defects and polymer-to-small molecule interfaces are all likely to provide bandgap states, however no significant distinction was seen between the electrical characteristics of the different films to enable them to be separated. The multiple temperature-dependent transport regimes seen in this study was also observed by Bourguiga et al. in a vapour-deposited octithiophene based transistors and has been attributed to a grain boundary-limited charge transport model.[37] Such a distinction cannot be made in our case, as the same temperature dependent transport regimes were also observed in the amorphous polymer PTAA device. It may be that grain boundaries in the blend films become transport limiting at a lower temperature than was investigated in this study, however we have recently seen evidence that grain boundaries in this system provide less of a barrier to hole transport than has been observed in single component systems.[17]

4. Conclusion

In conclusion, we have shown that finding an optimized ratio of semiconductor components is critical for maximising the hole mobility in this binary organic small molecule : polymer semiconducting blends and transistors. Energy filtered TEM studies combined with lateral conductivity mapping of the blend transistor channels was used to obtain the first direct evidence of the evolution of hole transport as a function of film composition. Through the use of low temperature transport measurements we were able to demonstrate that charge transport in these organic blend transistors is starkly different to that observed in single material (either diF-TES ADT or PTAA) based devices. Finally, we demonstrated the effect of blending organic semiconductors on the resulting bandgap trap distributions and laid out a framework for the improvement of such devices.

5. Experimental Section

Transistor Fabrication: Top-gate bottom-contact TFTs were fabricated on glass substrates with thermally evaporated 5 nm Al, 25 nm Au source and drain electrodes. The Al underlayer provides improved adhesion to the glass. These source and drain electrodes were treated with a pentafluorobenzenethiol monolayer by immersion in an IPA solution. The blend devices were fabricated by spin casting films of diF-TES ADT and PTAA in various ratios, from a solution using tetralin as the solvent. For pristine devices, the diF-TES ADT and PTAA single components were spin cast from a chloroform solution. All films were dried at 100 °C for 10 minutes to remove remaining solvent. After semiconductor deposition, a 900 nm layer of cytop was deposited as a dielectric, the devices were then annealed at 100 °C for a further 10 minutes. Finally, Al top gates were deposited by thermal evaporation. For samples studied by conductive AFM, the same fabrication method was conducted, excepting the cytop and gate electrode depositions. The source electrode was then contacted with silver paste and copper wire to connect with the atomic force microscope.

Materials Characterisation: Conductive atomic force microscopy measurements were carried out using an Agilent 5500 scanning probe microscope operating in contact mode. Mikromasch CSC11/Ti-Pt probes were used which were platinum coated for electrical conductivity and had spring constants of 0.5–6 N/m. A bias of +10 V was applied to the source electrode, while the conductive tip was held at ground, enabling hole injection from the electrode and extraction through the tip.

Energy-filtered TEM (EF-TEM) experiments were examined with a Zeiss Libra 120 at 120kV using a conventional three-window method. A typical energy width was 15eV. An emission current as low as 3μA and minimal exposure times were used to minimize electron-beam-induced sample damage, along with frequent morphology monitoring before and after elemental mapping. Thickness maps were obtained along with 0eV (elastic) images and S maps by calculating the intensity ratio of filtered and unfiltered images, yielding pixel-by-pixel t/λ values. (The film thickness t is in nanometer, and λ is an unknown constant representing the mean free path of electrons in the sample film.)

TFT Characterisation: Electrical measurements were conducted in nitrogen at room temperature, using an Agilent B2902A parameter analyser, while low temperature measurements were conducted under vacuum using a Keithley 4200 parameter analyser.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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